REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	25 March 1997	Final 26 May 93 - 31 Dec 96

4. TITLE AND SUBTITLE
Models of Multiprocessor Architectures and Algorithms (Final Report)

5. FUNDING NUMBERS
DAAH 04-93-G-0229

6. AUTHOR(S)
Eric E. Johnson

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
New Mexico State University
Las Cruces, NM

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
U.S. Army Research Office
P. O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
ARO 30953.9-EL-H

11. SUPPLEMENTARY NOTES
The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

A key requirement for the effective use of multiprocessors in real-world applications is an ability to accurately predict the performance of a specific algorithm on a specific architecture. This research developed such a prediction methodology, which permits separate evaluation of algorithm and architecture performance, with only a small number of "cross" parameters required to link the models. Additional results include program behavior models that lead to effective trace compression techniques.

20010301 140

14. SUBJECT TERMS
Computer architecture, performance modeling, performance prediction, parallel computing, multiprocessor, traces

15. NUMBER OF PAGES
4

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

Models of Multiprocessor Architectures and Algorithms

Final Report

Eric E. Johnson

25 March 1997

U.S. Army Research Office

Grant # DAAH04–93–G–0229

New Mexico State University

Approved for public release; distribution unlimited.

The views, opinions, and findings contained in this report are those of the author and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

Statement of the Problem Studied

A key requirement for the effective use of multiprocessor systems in real-world applications is an ability to accurately predict the performance of a specific algorithm on a specific architecture. Such performance prediction tools assist the system designer in initially selecting suitable algorithms and architectures, and then in modifying them to improve performance.

Existing techniques for joint performance prediction of multiprocessor algorithms and architectures generally require joint *evaluation* of the model for each algorithm/architecture pair of interest. This results in significantly more computation than an approach that models algorithms and architectures separately, with joint performance computed from the individual performance measures. In addition, the accuracy of current techniques is often affected by assumptions about algorithm and architectural behavior for which few measurements have been available.

The objective of this research was to extend our previous work in modeling multiprocessor and distributed system performance to produce an efficient, accurate performance prediction methodology applicable to Army systems. This technique is based upon measurements of important applications, and permits separate evaluation of algorithm and architecture performance with only a small number of "cross" parameters required to link the two models.

Specific Aims: Measure the characteristics of parallel computer programs of the types used in Army systems, validate a theoretical model of parallel computer system performance, establish a data base of parallel computing performance measurements for Internet access.

Findings: Researchers supported by this contract developed the following:

1. An efficient, accurate methodology for predicting the performance of algorithms on parallel architectures. This methodology was validated both in our own work and by outside researchers.
2. A parallel algorithm for tracking multiple targets in video imagery that is portable among nearly all parallel architecture classes, and that scales well from small to large multiprocessors. Apart from its direct utility in Army programs, this algorithm is a useful vehicle for validating our performance prediction model over a very wide range of parallel machines.
3. A portable parallel architecture simulator and cache simulator.
4. A model of redundancy in instruction and data traces that can be applied to reduce trace sizes by up to two orders of magnitude. The significance of the later result is evident in the widespread use of our PDATS trace format in the computer architecture community.
5. A database of uniprocessor and multiprocessor traces that is in use by researchers worldwide.
6. Hardware to capture complete and filtered traces in real time from uniprocessors and multiprocessors.

This body of work is cited internationally in online references used by the research community (e.g.:
http://www.hensa.ac.uk/parallel/simulation/architectures/pdats/index.html,
http://www.hensa.ac.uk/parallel/acronyms/index.html,
http://www.cs.newcastle.edu.au/Research/VRMG/index.html).

Manuscripts Submitted

E. E. Johnson, J. Ha, and M. B. Zaidi, "Lossless Trace Compression," submitted to *IEEE Transactions on Computers*.

D. Ma, E.E. Johnson, J. Ramirez-Angulo, and A. de Luca, "A New Hardware Algorithm for Computing Object Centers," submitted to *IEEE Transactions on Solid-State Circuits*.

Publications and Technical Reports

E.E. Johnson, "Independent Performance Modeling of Parallel Architectures and Algorithms," 1993 International Conference on Computing and Information, IEEE Computer Society Press. (also published as Technical Report NMSU-ECE-93-001, January '93).

E. E. Johnson, R. S. Moore, J. T. Polson, "A Data Structure for Virtual Memory Management in 'A Research GMMP Operating System'," Technical Report NMSU-ECE-93-017, July 1993.

E. E. Johnson and C. D. Schieber, "RATCHET: Realtime Address Trace Compression Hardware for Extended Traces," Technical Report NMSU-ECE-93-018.

E. E. Johnson and J. Ha, "PDATS: Lossless Address Trace Compression for Reducing File Size and Access Time," proceedings of 1994 IEEE International Phoenix Conference on Computers and Communications, IEEE, 1994.

C. C. Weng and E. E. Johnson, "The Time-Space Model for Instruction Reference Behavior," proceedings of 1994 IEEE International Phoenix Conference on Computers and Communications, IEEE, 1994.

E. E. Johnson and C. D. Schieber, "RATCHET: Realtime Address Trace Compression Hardware for Extended Traces," ACM Performance Evaluation Review (refereed), vol. 21, no. 3, pp. 22-32, April 1994.

E. E. Johnson and S. Tatineni, "Investigation of a Variation on Working Set Prefetching," Technical Report NMSU-ECE-94-007, July 1994.

S. Das and E.E. Johnson, "Accuracy of Filtered Traces," proceedings of 1995 IEEE International Phoenix Conference on Computers and Communications, IEEE, 1995.

E. E. Johnson, *et al.*, "Evaluation of Futurebus+ for a GMMP Multiprocessor," in *Advanced Multi-microprocessor Bus Architectures*, Janusz Zalewski, ed., pp 376-379, IEEE Computer Society Press, 1995.

E. E. Johnson, "Graffiti on 'The Memory Wall'," *Computer Architecture News*, Association for Computing Machinery, September, 1995.

B. Hunt and E. E. Johnson, "Multiprocessor Memory Management: Integrating Four-Address Virtual Memory and Aliased Page Tables," *Proceedings of 1996 IEEE International Phoenix Conference on Computers and Communications*, IEEE, 1996.

D. Ma, E.E. Johnson, J. Ramirez-Angulo, and A. de Luca, "A New Hardware Algorithm for Computing Object Centers," *Proceedings, 1996 Midwest Symposium on Circuits and Systems*, August 1996.

Scientific personnel supported by this project and **degrees awarded**:

		1993	1994	1995	1996	Degree
PI:	Eric Johnson	•	•	•	•	
Students:	Stan Dixon			•		MSEE student
	Bryan Hunt	•	•	•		MSEE granted
	Ding Ma	•	•	•		Ph.D. student
	Praveen Mamnani		•	•		BSCS granted
	Alan Taylor	•	•	•		Ph.D. student
	Baqar Zaidi			•		MSEE granted
	Che-Chi Weng	•				Ph.D. received
	Kevin Sitze	•	•			MSEE granted
	Sudhan Das	(supported by related equipment grant)				MSEE granted
	Roy Moore	(supported by related AASERT grant)				Ph.D. student